MORNING

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[Total No. of Questions: 09] [Total No. of Pages: 2]

Uni. Roll No. .....

Program/Course: B.Tech. (Batch 2018 Onwards)
Semester: 3rd
Name of Subject: Digital Electronics
Subject Code: PCEC-104
Paper ID: 16034
Scientific calculator is allowed

Time Allowed: 3 Hours **Max. Marks: 60**

NOTE:

1) Part A and B is compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice.
3) Any missing data may be assumed appropriately.

Part-A

[Marks: 02 each]

Q1.

(a) Explain the advantages of TTL over DTL.
(b) Give the comparison between combinational and sequential circuits.
(c) How the latch is different from Flip-flop?
(d) Define trailing-edge triggering?
(e) Draw the logic diagram for the logic function Y = (A+B+C).D
(f) Solve the following:
$(378.93)_{10}$ to Octal
$(5C7)_{16}$ to Decimal

Part-B

[Marks: 04 each]

Q2. Explain how a 4 bit data is entered and taken out in PISO register. Draw the block diagram and timing diagram for the same.

Q3. Explain the principle of operation and working of Counter type ADC along with proper diagram.

Q4. Define race around condition in Flip Flops and how can it be eliminated?

Q5. Solve the following:

i. Subtract 14 from 46 using 2's complement method.
ii. Add -75 to +26 using 2's complement method.

P.T.O.

Q6. Design a full adder using logic gates by solving with K-map along with the truth table.

Q7. Minimize the following logical expression using Boolean algebra:

i. (A+C)(A+D)(B+C)(B+D)
ii. (AB+C)(AB+D)

Part-C **[Marks: 12 each]**

Q8. (a) Explain the Working of a Successive approximation A/D Converter with the help of a suitable diagram and compare its performance in terms of speed, accuracy and resolution with other ADCs.

OR

(b). Explain in detail the working of BCD to excess-3 convertor by writing the minimized logical expression for every output of truth table solved through k-Maps and implement the circuit using logic gates.

Q9. (a) Solve the following with K-map and also implement using logic gates.

$F(A,B,C,D,E) = \Sigma m\,(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$

OR

(b) Design 3-bit synchronous binary counter using JK flip flop for memory element.